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EXAMINER	
RYMAN, DANIEL J	

ART UNIT	PAPER NUMBER
2665	

DATE MAILED: 01/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/816,242	PECHNER ET AL.	
	Examiner	Art Unit	
	Daniel J. Ryman	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25 and 27-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25 and 27-36* is/are rejected.

7)☒ Claim(s) *21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Examiner acknowledges Applicant's filing of an RCE on 11/21/2005.

2. Applicant's arguments with respect to claims 1-25 and 27-36 have been considered but are moot in view of the new ground(s) of rejection.

Specification

3. Examiner requests that Applicant update the application information seen on page 1, lines 9-23 of the specification in order to reflect any changes in the status of the applications.

Claim Objections

4. Claim 21 is objected to because of the following informalities: in line 13 "the recovered data" should be "the intermediate-speed data channels". Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-25 and 27-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Obana et al. (USPN 5,001,711) in view of Yamato et al. (USPN 6,041,062), previously presented, in further view of Shibagaki et al. (USPN 4,704,715), previously presented.

7. Regarding claims 1 and 21, Obana teaches receiving a tributary (DS3) complying with a jitter tolerance (Fig. 5; col. 5, lines 6-23; and col. 6, lines 57-64) where the elimination of jitter in the signal evinces that the system is concerned with jitter such that the tributary complies with

jitter requirements when received and the system ensures that the tributary continues to do so as the tributary passes through the system; recovering data from the tributary (Fig. 5 and col. 5, lines 6-23); receiving a reference clock (col. 5, lines 40-54); converting the recovered data into at least two intermediate-speed data channels (DS2 signals), wherein each intermediate-speed data channel is timed by a first clock based on the reference clock (Fig. 5 and col. 5, lines 6-54); converting each intermediate-speed data channel into at least two low-speed data channels (DS1 signals), wherein the low-speed data channels in aggregate contain the recovered data and each low-speed data channel is timed by a second clock based on the reference clock (Fig. 5 and col. 5, lines 6-54).

Obana does not expressly disclose that the system operates in an optical fiber communication system. Yamato teaches, in a multiplexing system, multiplexing low-speed optical signals into high-speed optical signals and demultiplexing high-speed optical signals into low-speed optical signals in order to interface high-speed and low-speed optical networks to each other (col. 1, lines 7-18). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have the system operate in an optical fiber communication system in order to interface high- and low- speed optical networks to each other.

Obana in view of Yamato does not expressly disclose modulating each low-speed data channel to generate a corresponding low-speed symbol channel; and frequency division multiplexing the low-speed symbol channels to produce an electrical high-speed channel for transmission in optical form across the communications system. Shibagaki teaches, in an optical communication system, that it is well known in the art to use a frequency division multiplexing scheme in order to improve the transmission efficiency of the different signals over the optical

fiber (col. 1, lines 39-42). In order to use this scheme, Shibagaki teaches modulating the low-speed signals to obtain a low-speed channel located on a particular carrier frequency (Fig. 2 and col. 4, lines 44-56). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modulate each low-speed data channel to generate a corresponding low-speed symbol channel and to frequency division multiplex the low-speed symbol channels to produce a high-speed channel in order to improve the transmission efficiency of the different signals over the optical fiber.

8. Regarding claims 2 and 22, Obana in view of Yamato in further view of Shibagaki discloses that the tributary and the jitter tolerance conform to a SONET protocol (Yamato: col. 1, lines 13-18).

9. Regarding claims 3 and 23, Obana in view of Yamato in further view of Shibagaki discloses that each low-speed data channel includes: a frequency header and a data rate which conforms to the SONET protocol (Yamato: col. 1, lines 13-18); and a payload which does not conform to the SONET protocol (VT or VC signal) (Yamato: col. 4, lines 58-col. 5, line 5 and col. 7, lines 35-50).

10. Regarding claims 4, 5, 24, and 25, Obana in view of Yamato in further view of Shibagaki discloses that each low-speed data channel includes: a frequency header and a data rate which conforms to the STS-1 protocol (Yamato: col. 5, lines 8-10); and a payload which does not conform to the STS-1 protocol (VT or VC signal) (Yamato: col. 4, lines 58-col. 5, line 5 and col. 7, lines 35-50). Obana in view of Yamato in further view of Shibagaki does not expressly disclose that the STS-1 signal is an STS-3 signal or an STS-48 signal. However, it is generally considered to be within the ordinary skill in the art to adjust, vary, select, or optimize the

numerical parameters or values of any system absent a showing of criticality in a particular recited value. The burden of showing criticality is on applicant. In re Mason, 87 F.2d 370, 32 USPQ 242 (CCPA 1937); Marconi Wireless Telegraph Co. v. U.S., 320 U.S. 1, 57 USPQ 471 (1943); In re Schneider, 148 F.2d 108, 65 USPQ 129 (CCPA 1945); In re Aller, 220 F.2d 454, 105 USPQ 233 (CCPA 1055); In re Saether, 492 F.2d 849, 181 USPQ 36 (CCPA 1974); In re Antonie, 559 F.2d 618, 195 USPQ 6 (CCPA 1977); In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). Since Obana in view of Yamato in further view of Shibagaki discloses that the STS signal is an STS-1 signal, it would have been obvious to vary the rate of the STS signal to STS-3 or STS-48, absent a showing of criticality by Applicant.

11. Regarding claim 6, Obana in view of Yamato in further view of Shibagaki discloses that the step of converting the recovered data into at least two intermediate speed data channels comprises: recovering a clock from the tributary (Obana: col. 5, lines 40-54 and Yamato: col. 2, lines 24-47 and col. 10, lines 33-40); phase aligning the reference clock to the recovered clock (Yamato: col. 2, lines 24-47 and col. 10, lines 33-40); retiming the recovered data using the phase-aligned reference clock (Yamato: col. 2, lines 24-47; col. 7, lines 15-34; and col. 10, lines 33-40); and time division demultiplexing the retimed, recovered data into the intermediate-speed data channels (Obana: col. 5, lines 16-23 and Yamato: col. 4, lines 38-54; col. 5, lines 6-13; and col. 7, lines 15-34).

12. Regarding claim 7, Obana in view of Yamato in further view of Shibagaki discloses that the step of converting each intermediate-speed data channel into at least two low-speed channels comprises: dividing the phase-aligned reference clock to produce the first clock (Obana: col. 5, lines 40-54); retiming the recovered data in the intermediate-speed data channels using the first

clock (Obana: col. 5, lines 40-54 and Yamato: col. 2, lines 24-47; col. 7, lines 15-34; and col. 10, lines 33-40); time division demultiplexing the intermediate-speed data channels into the low-speed data channels (Obana: col. 5, lines 16-23 and Yamato: col. 4, lines 38-54; col. 5, lines 6-13; and col. 7, lines 15-34).

13. Regarding claims 8 and 27, Obana in view of Yamato in further view of Shibagaki discloses converting the electrical high-speed channel to an optical high-speed channel (Yamato: col. 8, lines 15-23); transmitting the optical high-speed channel across a fiber (Yamato: col. 8, lines 15-23); receiving the optical high-speed channel (Yamato: col. 8, lines 24-34); converting the received optical high-speed channel to a receive-side electrical high-speed channel (Yamato: col. 8, lines 24-34); frequency division demultiplexing the receive-side electrical high-speed channel into at least two receive-side low-speed symbol channels (Yamato: col. 8, lines 24-34 and Shibagaki: Fig. 2; col. 1, lines 39-42; and col. 4, lines 44-56); demodulating each receive-side low-speed symbol channel to generate a corresponding receive-side low-speed data channel (Shibagaki: Fig. 2; col. 1, lines 39-42; and col. 4, lines 44-56); recovering a clock and data from each receive-side low-speed data channel (Yamato: col. 2, lines 24-47 and col. 10, lines 33-40); generating a receive-side reference clock synchronized to the receive-side recovered data (Obana: col. 5, lines 8-15 and col. 5, lines 26-39 and Yamato: col. 2, lines 24-47; col. 7, lines 15-34; and col. 10, lines 33-40); converting the receive-side low-speed data channels (DS1 signals) into at least two receive-side intermediate-speed data channels (DS2 signals) (Obana: col. 5, lines 8-15 and col. 5, lines 26-39); and converting the receive-side intermediate-speed data channels (DS2 signals) into a receive-side tributary (DS3 signals) (Obana: col. 5, lines 8-15 and col. 5, lines 26-39), wherein the receive-side tributary contains all of the receive-side recovered

data, and the receive-side tributary is timed by a clock based on the receive-side reference clock and complies with the jitter tolerance (Obana: col. 5, lines 8-15; col. 5, lines 26-39; and col. 6, lines 57-64 and Yamato: col. 4, lines 38-54; col. 5, lines 6-13; and col. 7, lines 15-34).

14. Regarding claims 9 and 28, Obana in view of Yamato in further view of Shibagaki discloses that the tributary, the receive-side tributary and the jitter tolerance conform to a SONET protocol (Yamato: col. 1, lines 13-18).

15. Regarding claim 10, Obana in view of Yamato in further view of Shibagaki discloses that the step of converting the receive-side low-speed data channels into at least two receive-side intermediate-speed data channels comprises: storing the recovered data from each receive-side low-speed data channel (Obana: col. 5, lines 6-15) where it is implicit that the data is stored; aligning a timing for the receive-side low-speed data channels (Obana: col. 7, lines 50-57 and col. 8, lines 5-20); and time division multiplexing the receive-side recovered data from the receive-side low-speed data channels into the at least two receive-side intermediate-speed data channels according to the aligned timing (Obana: col. 5, lines 6-15 and col. 5, lines 26-39).

16. Regarding claim 11, Obana in view of Yamato in further view of Shibagaki discloses that the step of converting the receive-side intermediate-speed data channels into the tributary comprises: storing the recovered data from each receive-side intermediate-speed data channel (Obana: col. 5, lines 6-15) where it is implicit that the data is stored; aligning a timing for the receive-side intermediate-speed data channels (Obana: col. 7, lines 50-57 and col. 8, lines 5-20); and time division multiplexing the stored recovered data from the receive-side intermediate-speed data channels according to the aligned timing (Obana: col. 5, lines 6-15 and col. 5, lines 26-39).

17. Regarding claims 12 and 30, Obana discloses recovering data from each low-speed data channel (DS1 signals) (Fig. 5 and col. 5, lines 6-15); generating a reference clock synchronized to the recovered data (col. 5, lines 26-39); and converting the low-speed data channels into at least two intermediate-speed data channels (DS2 signals) (Fig. 5 and col. 5, lines 6-15); and converting the intermediate-speed data channels into a tributary (DS3 signals), wherein the tributary contains all of the recovered data (Fig. 5 and col. 5, lines 6-15), and the tributary is timed by a clock based on the reference clock and complies with the jitter tolerance (col. 5, lines 26-39 and col. 6, lines 57-64).

Obana does not expressly disclose that the system operates in an optical fiber communication system. Yamato teaches, in a multiplexing system, multiplexing low-speed optical signals into high-speed optical signals and demultiplexing high-speed optical signals into low-speed optical signals in order to interface high-speed and low-speed optical networks to each other (col. 1, lines 7-18). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have the system operate in an optical fiber communication system in order to interface high- and low- speed optical networks to each other.

Obana in view of Yamato does not expressly disclose frequency division demultiplexing an electrical high-speed channel into at least two low-speed symbol channels or demodulating each low-speed symbol channel to generate a corresponding low-speed data channel. Shibagaki teaches, in an optical communication system, that it is well known in the art to use a frequency division multiplexing scheme in order to improve the transmission efficiency of the different signals over the optical fiber (col. 1, lines 39-42). In order to use this scheme, Shibagaki teaches modulating the low-speed signals to obtain a low-speed channel located on a particular carrier

frequency (Fig. 2 and col. 4, lines 44-56). It is implicit that in order to recover the original signal the reverse process will occur, namely demultiplexing and demodulating. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to demultiplex the electrical high-speed channel into at least two low-speed symbol channels and to demodulate each low-speed symbol channel to generate a corresponding low-speed data channel in order to improve the transmission efficiency of the different signals over the optical fiber.

18. Regarding claims 13 and 31, Obana in view of Yamato in further view of Shibagaki discloses that the tributary and the jitter tolerance conform to a SONET protocol (Yamato: col. 1, lines 13-18).

19. Regarding claims 14 and 32, Obana in view of Yamato in further view of Shibagaki discloses that each low-speed data channel includes: a framing header and a data rate which conforms to the SONET protocol (Yamato: col. 1, lines 13-18); and a payload which does not conform to the SONET protocol (VT or VC signal) (Yamato: col. 4, lines 58-col. 5, line 5 and col. 7, lines 35-50).

20. Regarding claims 15, 16, 33, and 34, Obana in view of Yamato in further view of Shibagaki discloses that each low-speed data channel includes: a frequency header and a data rate which conforms to the STS-1 protocol (Yamato: col. 5, lines 8-10); and a payload which does not conform to the STS-1 protocol (VT or VC signal) (Yamato: col. 4, lines 58-col. 5, line 5 and col. 7, lines 35-50). Obana in view of Yamato in further view of Shibagaki does not expressly disclose that the STS-1 signal is an STS-3 signal or an STS-48 signal. However, it is generally considered to be within the ordinary skill in the art to adjust, vary, select, or optimize the numerical parameters or values of any system absent a showing of criticality in a particular

recited value. The burden of showing criticality is on applicant. In re Mason, 87 F.2d 370, 32 USPQ 242 (CCPA 1937); Marconi Wireless Telegraph Co. v. U.S., 320 U.S. 1, 57 USPQ 471 (1943); In re Schneider, 148 F.2d 108, 65 USPQ 129 (CCPA 1945); In re Aller, 220 F.2d 454, 105 USPQ 233 (CCPA 1055); In re Saether, 492 F.2d 849, 181 USPQ 36 (CCPA 1974); In re Antonie, 559 F.2d 618, 195 USPQ 6 (CCPA 1977); In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). Since Obana in view of Yamato in further view of Shibagaki discloses that the STS signal is an STS-1 signal, it would have been obvious to vary the rate of the STS signal to STS-3 or STS-48, absent a showing of criticality by Applicant.

21. Regarding claims 17 and 35, Obana in view of Yamato in further view of Shibagaki discloses that the step of converting the low-speed data channels into at least two intermediate-speed data channels comprises: storing the recovered data from each low-speed data channel (Obana: col. 5, lines 6-15) where it is implicit that the data is stored and where buffers are a well-known device for storing data; aligning a timing for the low-speed data channels (Obana: col. 7, lines 50-57 and col. 8, lines 5-20); and time division multiplexing the recovered data from the low-speed data channels into the at least two intermediate-speed data channels according to the aligned timing (Obana: col. 5, lines 6-15 and col. 5, lines 26-39).

With respect to claim 35, Obana in view of Yamato in further view of Shibagaki does not expressly disclose using a state machine for aligning the timing; however, Examiner takes official notice that state machines are a well-known programming technique. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a state machine for aligning the timing since state machines are a well-known programming technique.

22. Regarding claim 18, Obana in view of Yamato in further view of Shibagaki discloses that the step of aligning a timing for the low-speed data channels comprises: generating a framing pulse for each low-speed data channel; and aligning the framing pulses (Obana: col. 7, lines 50-57 and col. 8, lines 5-21).

23. Regarding claims 19 and 36, Obana in view of Yamato in further view of Shibagaki discloses that the step of converting the intermediate-speed data channels into the tributary comprises: storing the recovered data from each intermediate-speed data (Obana: col. 5, lines 6-15) where it is implicit that the data is stored and where buffers are a well-known device for storing data; aligning a timing for the intermediate-speed data channels (Obana: col. 7, lines 50-57 and col. 8, lines 5-20); and time division multiplexing the stored recovered data from the intermediate-speed data channels according to the aligned timing (Obana: col. 5, lines 6-15 and col. 5, lines 26-39).

With respect to claim 36, Obana in view of Yamato in further view of Shibagaki does not expressly disclose using a state machine for aligning the timing; however, Examiner takes official notice that state machines are a well-known programming technique. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a state machine for aligning the timing since state machines are a well-known programming technique.

24. Regarding claim 20, Obana in view of Yamato in further view of Shibagaki discloses that the step of aligning a timing for the intermediate-speed data channels comprises: generating a framing pulse for each intermediate-speed data channel; and aligning the framing pulses (Obana: col. 7, lines 50-57 and col. 8, lines 5-21).

25. Regarding claim 29, Obana in view of Yamato in further view of Shibagaki discloses that the first time-division multiplexer comprises: aligning a timing for the receive-side intermediate-speed data channels (Obana: col. 7, lines 50-57 and col. 8, lines 5-20); buffers for storing the recovered data from each receive-side intermediate-speed data channel and releasing the stored recovered data according to the aligned timing (Obana: col. 7, lines 50-57 and col. 8, lines 5-21) where it is implicit that the data is stored and where buffers are a well-known device for storing data; and multiplexers for combining the released data (Obana: col. 5, lines 6-15 and col. 5, lines 26-39); and wherein the second time-division multiplexer comprises: aligning a timing for the receive-side low-speed data channels (Obana: col. 7, lines 50-57 and col. 8, lines 5-20); buffers for storing the recovered data from each receive-side low-speed data channel and releasing the stored recovered data according to the aligned timing (Obana: col. 7, lines 50-57 and col. 8, lines 5-21) where it is implicit that the data is stored and where buffers are a well-known device for storing data; and multiplexers for combining the released data (Obana: col. 5, lines 6-15 and col. 5, lines 26-39).

Obana in view of Yamato in further view of Shibagaki does not expressly disclose using a state machine for aligning the timing; however, Examiner takes official notice that state machines are a well-known programming technique. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a state machine for aligning the timing since state machines are a well-known programming technique.

Conclusion

26. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Taylor (USPN 5,938,309) see entire document which pertains to a WDM system containing modulators.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel J. Ryman whose telephone number is (571)272-3152. The examiner can normally be reached on Mon.-Fri. 7:00-4:30 with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (571)272-3155. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Daniel J. Ryman
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